EE/CprE/SE 491 WEEKLY REPORT 06
Oct 29 – Nov 4

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - This week was focused on continuing to bring designs and modules, from both teammates and previous teams' files, into our tools to simulate and learn more about what methods might work. We also worked towards a more solidified list of requirements for our project, mostly by prioritizing the characterizations that we proposed to our client earlier, we are still working on getting feedback on which characterizations and tests are most desirable for our client.

- **Past week accomplishments**
  - Vinicius Malaman Soares: Created design with ReRAM cells but ran into ngspice errors. Looked into past teams' design choices and how they worked out.
  - Tyler Kloser: Work on setting up the VM so I can work remotely, Continue to test the capabilities of Magic
  - Ali Mannan: Made significant advancements on layout of 1T1R, fixed DRC issues with ReRAM, can connect ReRAM electrically to VDD, and then to the drain of the MOS.
  - Austin Miller: Imported 1T1R from previous team, briefly tried layout of 1T1R, worked on presentation for prioritizing characterization tests and requirements

- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: ReRAM cell does not seem to be well-supported by the pdk
  - Austin Miller: N/A
  - Vinicius Malaman Soares: Debug ngspice.

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Tyler Kloser	Downloaded the 1T1R cell, Worked on DRC errors with problems with my incorrect netlist	5	37
Ali Mannan	1T1R ReRAM cell layout advancement	6	47
Austin Miller	Brought 1T1R into magic (from previous team). Prioritized tests and characterizations for presenting to client to solidify our actual requirements	9	51
Vinicius Malaman Soares	Created test involving the ReRAM cell, research into past teams designs	5	42

- **Comments and extended discussion**
  - N/A

Plans for the upcoming week

- Ali Mannan: Finish 1T1R layout and simulate post layout behavior with parasitics extracted
- Tyler Kloser: Decompose characteristic designs and design specific quantizations for primary goals
- Austin Miller: Bring some modules (ADC, DAC, etc.) from previous teams through parasitic extraction and design testbenches relating to the desired characterizations.
- Vinicius Malaman Soares: Debug ngspice errors, and finish tests involving the ReRAM

- **Summary of weekly advisor meeting**
  - Most of our discussion consisted of going over our proposed characterizations for feedback. This mostly boiled down to picking options from our list and organizing them into three goal categories: Primary (non-negotiable), Secondary, Tertiary (stretch). While we couldn't definitevly nail down the exact characterizations for each category of goals since our client was unable to make the meeting, we still left with a good idea for a couple of the most basic necessary modules and tests, namely those of basic cell modules like an array of individual 1T1R's (forming, setting, resetting of reram, varying sizes and endurance of reram cells), a single column of 1T1R's -- length undecided (IR droop, forming in column), and standalone mixed-signal blocks like an ADC, DAC, TIA, and MUX's (thermal noise, quantization error, offset). We also discussed potential constraints to be aware of for our project, like available pins, muxing, pad frame and IO restrictions, and internal vs. external control for certain designs due to physical limitations.